IN THE ABSTRACT:

The Abstract as amended below (with a replacement Abstract appended hereto - see end of amendment) shows added text with underlining and deleted text with ~~strikethrough~~.

Please DELETE the Abstract in its entirety and substitute the attached new Abstract.

ABSTRACT

The present invention relates to a method of circuit verification in digital design and in particular, relates to a method of register transfer level property checking to enable the same. Today's electrical circuit designs frequently contain up to several million transistors, and circuit designs need to be checked to ensure that circuits operate correctly. Formal methods for verification are becoming increasingly attractive since they confirm design behaviour without exhausting simulating a design. ~~The present invention provides a~~ A digital circuit design verification method ~~wherein~~, prior to a property checking process for each property of a non-reduced RTL model, ~~a reduced RTL model is determined~~ determines a reduced RTL model~~,~~ ~~which reduced RTL model~~ which retains specific signal properties of a non-reduced RTL model which are to be checked. A linear signal width reduction causes an exponential reduction of the induced state space. Reducing state space sizes in general goes hand in hand with reduced verification runtimes, ~~and~~ thus speeding up verification tasks.